

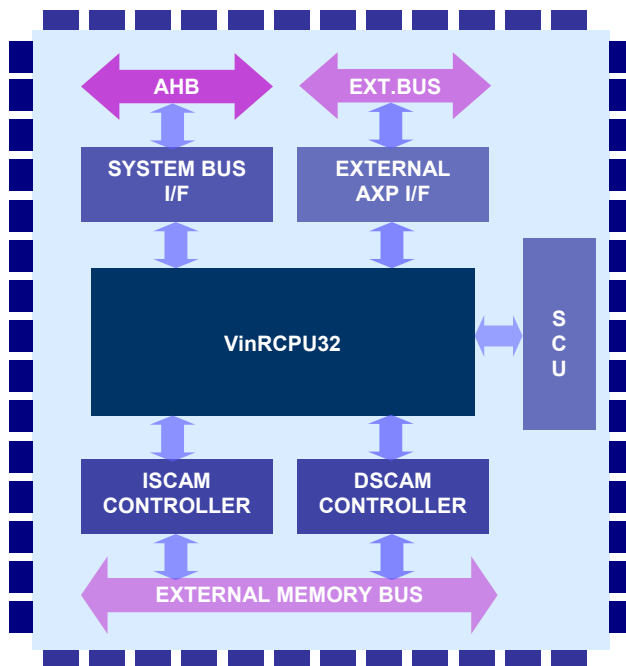
VinRZ5110

VinRZ5110 is a low power, high performance 32-bit processor solution targeting embedded applications where low power and system cost are of utmost importance. It is based on Harvard architecture, with single cycle memory access and multiple enhanced features as described below.

This processor system enables SoC designers to concentrate on design issues unique to their system. **VinRZ5110** is a *technology independent synthesizable macro*, highly portable across processes and can be easily integrated into system-on-chip designs.

Key Enhanced Features

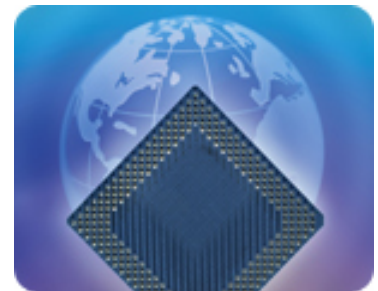
- **Five operating modes with optimized shadow register bank structure**
- Supports very fast context switching for high priority interrupt modes
- **Single cycle 32X16 MAC enabling convergence of RISC and DSP**
- Enables DSP applications
- **Native bus interface support for on-chip peripherals**
- Realizes low interrupt latencies
- **Memory copy, atomic memory access, semaphore instructions**
- Improves code density by a large margin
- **Low Power Modes support**
- Power-down mode (triggered by *en_idle* instruction)
- Supports low power modes that facilitate CE designs



VinRZ5110 Block Diagram

Processor Highlights

- Technology Independent synthesizable soft core
- Includes 32-bit, 5-stage Pipelined RISC CPU VinRCPU32
- Support for DSP instructions
- Saturated Addition
- Saturated Subtraction
- Integer Multiply
- Multiply-accumulate
- Byte, bit reversal instructions
- Achieves faster bit manipulation times- advantageous for mobile applications
- Immediate branch instruction with single cycle penalty
- 3-level fixed priority asynchronous Vectored Interrupt scheme
- Single cycle instruction & data memory access
- Support for up to 8 auxiliary processors
- Support for external interrupt controller
- AHB compliant System Bus Interface



VinChip Systems Inc

VinRZ5110

VinRZ5110 comprises the *VinRCPU32 Core, Single cycle access Instruction and Data Memory(SCAM) controllers, system control unit(SCU), external Auxiliary processor(AXP) interface and the System Bus Interface(SBI).*

VinRCPU32 Core

The 32-bit RISC CPU core features a 32x16 bit MAC capable of single cycle MAC operations, which enhances execution times of DSP instructions that are critical to DSP applications. The 32 bit datapath has been designed to minimize data, branch and structural hazard-related stalls. It can operate in five operating modes and has a shadow register bank, that provides fast context switching for high priority interrupts.

SCAM Controllers

The single cycle access memory interfaces enable single cycle access of data and instruction memories without incurring the power and time penalties of accessing the system bus, while having a lower area overhead than cached memory systems.

SBI

The System Bus Interface enables the processor to communicate with external peripherals through the AHB. The write and pre-fetch buffers in the SBI greatly boost the system throughput.

SCU

Primary auxiliary processor with register sets that control the operation of the processor such as power modes, buffers/SCAM controllers enable/disable, exception vector table selection and address alignment checking.

AXP I/F

Through this Auxiliary Processor interface, external auxiliary processors can be connected that can be used to extend the instruction set and realize hardware acceleration specific to the application.



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